U11 = 011 X XX
U10 = 010 X XX

1. Bus contention every memory cycle due to using $\overline{WR}$ (U4, 1) to control bus direction.

2. More bus contention due to no $\overline{RFSH}$ taken into account.

3. More bus contention due to $\overline{BUZOFF}$ not taken into account.

4. Memory is no good without a way to access it.

5. Power supply suggestion - add on 7805s: These regulators need about a 3 V differential. 5V in will not yield 5V out.